REMARKS

The Office Action of August 3, 2007 has been carefully reviewed and the claims have been amended in response thereto.

Claim Objections

As the Examiner has correctly noted, "external random access memory" cannot include "nonvolatile memory" because implicitly the external random access memory cannot be used during execution of the bootstrap program. The Applicant has therefore amended claims 5 and 16 to indicate that the processing unit communicates with external nonvolatile memory without that memory being part of the "external memory".

Claim Rejections -- 35 U.S.C. §103

Claims 1-6, 8-16, 18-23 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Fullam in view of Gupta and Devereux.

Claims 1 and 12 have been further amended to indicate that only after execution of the bootstrap program (to determine the type of external memory) is external memory (for which the type is determined) connected. This corrects an unintended implication in the claim, as recognized by the Examiner, suggesting that the external memory can be connected or used before completion of the determination of the type of the external memory during the bootstrap procedure.

In light of this amendment, it is believed that the rejection over Fullam in view of Gupta and Devereux has been overcome. Fullam does not teach executing the bootstrap memory before "connecting to the external memory as will ultimately use the selected set up data for the reading and writing to the external memory" as now required by the claims. Instead, Fullam uses the external memory (albeit in a slow speed mode) in order to properly execute the bootstrap program to determine the memory's proper operating speed. Accordingly, a combination of Fullam and Gupta and Devereux fails to teach all the elements of the independent claims as now amended.

The Applicant further believes that Fullam does not teach the use of caches for execution of the bootstrap program before "write access to external memory for storage of data as necessary for the execution of the bootstrap program". This element is also required in all of the

claims. The Examiner doesn't cite the Fullam invention, in this case, but rather prior art mentioned in the background of Fullam. Yet this prior art uses a "fixed-parameter" architecture "having circuitry and software fixed in accordance with the specification of a particular external memory device". See column 3, lines 55-57 and Fig 1a (element 14) and Fig. 1b (element 30). Thus this prior art, while teaching caches, teaches away from systems that dynamically determines of the type of external memory to which they are connected, also required in the present invention.

The Applicant does not believe that any of these references fairly teach using a cache before there is access to external memory. Caches are by their nature intended for temporary storage of data that is obtained from, or being transferred to, external memory. Therefore, absent express teaching to the contrary, when there is description of a cache there is implicitly and external memory present and accessible. Again, because the Examiner relies on Fullam for the teaching of these claimed elements, a combination of Fullam and Gupta and Devereux must fail to teach all of the elements of the independent claims.

As noted in the previous response, the Applicant further believes that Fullam doesn't teach an "integrated processor without general purpose random access memory", a limitation in all claims, and a limitation for which Fullam is relied upon. A person of ordinary skill in the art would understand Fullam's execution unit 52 or some other on-board device, to implicitly include at least some general purpose random access memory needed for program execution absent any other explanation.

For this reason, applicant believes, Fullam does not teach executing a bootstrap program using internal systems storage structures such as caches, buffers, or registers. A person of ordinary skill in the art would understand that Fullam uses conventional on-board random access memory for this purpose, even though this is not mentioned.

In addition, Fullam does not teach execution of the bootstrap program to determine memory set-up data before being able to write to the external memory. Fullam clearly teaches that external memory is fully readable and writable using a slow-speed protocol before memory setup data is obtained.

Allowable Subject Matter

The Examiner has indicated that claims 7 and 17 are allowable if rewritten in

independent form including all of the limitations of the base claims in any intervening claim. The Applicant has made the necessary amendments to claims 7 and 17 to put them independent form, but has also changed the phrase "cache memory" to "internal systems storage structure" in the final paragraph of these claims to match the phrasing used in the parent claim that embraces not only caches but also internal buffers and registers. It is believed that this amendment is consistent with the Examiner's allowance of these claims but the Applicant notes that this additional amendment has the effect of slightly enlarging the scope of the claims 7 and 17 over that which was allowed.

In light of these comments and remarks, it is respectfully submitted that rejection of the claims is overcome and allowance of claims 1-23 is respectfully requested.

Respectfully submitted,

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